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CIRCUIT DEVICE MANUFACTURING METHOD

DETAILED DESCRIPTION OF THE INVENTION

Field of the Invention

5 This invention relates to a circuit device manufacturing method, and particularly relates to a circuit device manufacturing method with which the adhesion of the component elements of a circuit device to each other is improved using plasma.

10 Description of the Related Art

 With the progress of employment of IC packages in portable equipment and compact, high-density-mounting equipment, the concepts of mounting are changing greatly from those of conventional IC packages. There is an art concerning a
15 semiconductor device employing a polyimide resin sheet, which is a flexible sheet, as an example of an insulating resin sheet .

 Fig. 13 shows a semiconductor device using a flexible sheet 50 as an interposer substrate. Fig. 13(A) is a plan view of this semiconductor device and Fig. 13(B) is a sectional view
20 along line A-A of Fig. 13(B). A method of manufacturing this semiconductor device shall now be described.

 First, copper foil patterns 51 are prepared and adhered via an adhesive agent onto flexible sheet 50. Copper foil

patterns 51 comprises bonding pads 51A and islands 51B . Number and shape of foil patterns 51 depend on the variety of the element mounted thereon.

The symbol 52 indicates openings for leading out electrodes
5 from the rear surface of flexible sheet 50 and at these openings, the copper patterns 51 are exposed. Flexible sheet 50 is then conveyed to a die bonder and semiconductor elements 53 are mounted. Thereafter, this flexible sheet 50 is conveyed to a wire bonder and bonding pads 51A are electrically connected
10 with the pads of semiconductor elements 53 by metal wires 54.

Lastly, sealing is carried out by providing a sealing resin layer 55 on the top surface of flexible sheet 50 as shown Fig. 13(A) . Here, transfer molding is performed so as to cover bonding pads 51A, islands 51B, semiconductor elements 53, and
15 metal wires 54. Thereafter, soft solders, solder balls, or other connection means 56 are provided as shown in Fig. 13(B) , and by passage through a solder reflow furnace, spherical solders 56, which are fused with bonding pads 51A via openings 52, are formed. Thereafter, since semiconductor elements 53 are formed
20 in matrix form on flexible sheet 50, dicing is performed for separation into individual devices.

However, the semiconductor device manufacturing method described with reference to Fig. 13 had several problems due

to the employment of flexible sheet 50. That is, since flexible sheet 50 itself is of some thickness, there was a limit as to how thin a device could be made. In addition, cracks formed in flexible sheet 50 and flexible sheet 50 became warped in
5 the manufacturing process.

In order to resolve such problems as the above, a thin circuit device, with which an interposer substrate, such as flexible sheet 50, etc., is made unnecessary, and a method of manufacturing such a circuit device have been proposed.

10 Such a circuit device 60 shall now be described in outline with reference to Fig. 14. This circuit device 60 is configured without a flexible sheet or other interposer. By etching conductive films adhered in sheet-like form onto the top and rear of an insulating resin 62, a multilayer wiring structure,
15 comprising a first conductive wiring layer 63 and a second conductive wiring layer 64, is realized. First conductive wiring layer 63 and second conductive wiring layer 64 are insulated by an interlayer insulating layer 62 and are electrically connected at desired locations by multilayer
20 connection means 72. Also, external electrodes 74 are formed at desired locations of second conductive wiring layer 64, and these become the electrodes for connection with a mounted substrate, etc. On top of first conductive wiring layer 63,

an overcoat resin 76 is coated at locations besides locations that are to become pads, a semiconductor element 67 is affixed via an insulating adhesive agent 68, and the electrodes of semiconductor element 67 are electrically connected with first
5 conductive wiring layer 63 by means of metal wires 71. Sealing resin layer 73 has the function of sealing semiconductor elements 67 and metal wires 71 and mechanically supporting the entirety.

The above-described circuit device 60 is configured without a flexible sheet or other interposer and has the merit
10 that the overall device is thereby made thin, etc.

As an art for removing contaminants attached to the top surfaces of patterns formed of metal, there is the art of plasma irradiation. A method of irradiating plasma onto a lead frame, on which a semiconductor element is mounted, to remove
15 contaminants attached to the top surface shall now be described with reference to Fig. 15.

The configuration of a lead frame 110, which has been subject to a lead frame processing step, an element mounting step, etc., shall now be described with reference to Fig. 15 (A).
20 A semiconductor element 112 is mounted onto an island 114, which has been formed to a land form, and a plurality of leads 111 are disposed so as to surround island 114. Leads 111 correspond to electrodes provided on the top surface of semiconductor

element 112 and the respective electrodes are electrically connected via metal wires 113 to leads.

The plasma irradiation step shall now be described with reference to Fig. 15(B). First, lead frame 110 is set in a sealed container. Gas is then introduced into the container and plasma gas is generated by a discharge. The top surface of lead frame 110 is cleaned by the collision of radicals or ions existing in the plasma gas with the top surface of lead frame 110.

However, with the above-described circuit device 60, the adhesion of overcoat resin 76 to sealing resin layer 73 is not adequate and cracks form at the interface of the two components due to the thermal stress arising from temperature changes under usage conditions. There are also problems of entry of moisture, etc., contained in external air, into the circuit device from the interface between overcoat resin 76 and sealing resin layer 73.

Also, with the method of cleaning a lead frame by plasma irradiation as shown in Fig. 15, since complex shapes are formed so as to form island 114 and leads 111, the plasma irradiation causes localized increases in electric potential to occur in lead frame 110. There was thus the problem of current flowing into semiconductor element 112 via metal wires 113 due to such

localized potential differences in the lead frame and damaging a CMOS and other elements formed on the top surface of the semiconductor element. There was also the problem that, due to lead frame 110 becoming high in temperature in the plasma irradiation step, the leads become deformed and metal wires 113 become disconnected.

This embodiment of the invention has been made in view of such problems, and a main object of this embodiment of the invention is to provide a circuit device manufacturing method, with which the adhesion force among the elements making up a circuit device is improved by the use of plasma irradiation.

SUMMARY OF THE INVENTION

This embodiment of the invention provides a circuit device manufacturing method comprising the steps of: forming conductive films that are laminated in multiple layers with interlayer insulating layers interposed in between; forming a conductive wiring layer by selective removal of the conductive film at the top surface; forming through holes in the interlayer insulating layers and forming connection means in the through holes to electrically connect the conductive wiring layer with the conductive film at the rear surface; affixing and electrically connecting circuit elements to the

conductive wiring layer; irradiating plasma onto the
conductive wiring layer, including the circuit elements; and
forming a resin layer so as to cover the circuit elements.
By roughening the conductive wiring layer by plasma irradiation,
5 the adhesion of the conductive wiring layer to the resin member
can be improved.

Furthermore, in the case where a resin is formed on top
of the conductive wiring layer, by roughening the resin, the
adhesion of the resin layer to the resin can be improved. Also,
10 since the conductive wiring layer is electrically connected,
the voltage that is charged up in the resin due to plasma
irradiation is released to the exterior via the conductive wiring
layer and the conductive film. Since the generation of
localized electric potential differences in the plasma
15 irradiation step can thus be restrained, the breakage of
semiconductor elements and other circuit elements can be
restrained.

With this embodiment, the adhesion force among elements
that constitute circuit device is improved by the use of plasma
20 irradiation, thereby enabling the reliability of the circuit
device to be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

Fig. 2 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

5 Fig. 3 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

Fig. 4 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

10 Fig. 5 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

Fig. 6 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

15 Fig. 7 is a sectional view(A) and a sectional view (B) showing a circuit device manufacturing method of preferred embodiment.

Fig. 8 is a sectional view (A) and a plan view (B) showing a circuit device manufacturing method of preferred embodiment.

Fig. 9 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

20 Fig. 10 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

Fig. 11 is a plan view showing a circuit device manufacturing method of preferred embodiment.

Fig. 12 is a sectional view showing a circuit device manufacturing method of preferred embodiment.

Fig. 13 is a plan view (A) and a sectional view (B) showing a related-art circuit device manufacturing method.

5 Fig. 14 is a sectional view showing a related-art circuit device manufacturing method.

Fig. 15 is a plan view (A) and a sectional view (B) showing a related-art circuit device manufacturing method.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A circuit device manufacturing method of preferred embodiment comprises the steps of: forming conductive films 23 that are laminated in multiple layers with interlayer insulating layers 22 interposed in between; forming a conductive wiring layer 12 by selective removal of conductive film 23 at
15 the top surface; forming through holes 31 in interlayer insulating layers 22 and forming connection means 14 in through holes 31 to electrically connect conductive wiring layer 12 with conductive film 23 at the rear surface; affixing and
20 electrically connecting circuit elements 13 to conductive wiring layer 12 at the rear surface; irradiating plasma onto conductive wiring layer 12, including circuit elements 13; and forming a sealing resin layer 17 so as to cover circuit elements

13. These respective steps shall now be described.

In the first step of this embodiment, conductive films 23 that are laminated in multiple layers with an interlayer insulating layer 22 interposed in between are prepared, a
5 conductive film 23 is removed selectively to form a conductive wiring layer 12, and through holes 31 are formed in interlayer insulating layer 22 and connection means 14 are formed in through holes 31 to electrically connect conductive wiring layer 12 with conductive film 23 as shown in Fig. 1 to Fig. 3.

10 In this step, first, an insulating sheet 21 is prepared in which a first conductive film 23A and a second conductive film 23B are laminated with an interlayer insulating layer 22 interposed in between. Here, a glass epoxy resin, a resin type resin, or a liquid crystal polymer may be cited as an example
15 of the material of interlayer insulating layer 22. First conductive film 23A is formed across practically the entirety of the top surface of insulating sheet 21 and second conductive film 23B is formed across practically the entirety of the rear surface. A thermoplastic resin or a thermosetting resin may
20 be used as the material of interlayer insulating layer 22. Also, first conductive film 23A and second conductive film 23B are preferably formed of Cu as the principal material or of a known lead frame material and are coated onto interlayer insulating

layer 22 by a plating method, vapor deposition method, or sputter method or are adhered as metal foils formed by a rolling method or plating method. Insulating sheet 21 may also be formed by a casting method. To briefly describe a method of manufacture thereof, first a paste-form insulating resin is coated onto first conductive film 23A, having the form of a flat film, and the paste-form insulating resin is also coated onto second conductive film 23B, having the form of a flat film. Insulating sheet 21 is then prepared by adhering these two parts together after semi-curing of the resin.

In the case of the casting method in which a sheet is formed upon coating of a paste-like substance, the film thickness of the sheet will be approximately 10 μ m to 100 μ m. In the case of forming as a sheet, the minimum film thickness of a commercially available product is 25 μ m. A filler may be mixed inside in consideration of thermal conductivity. Glass, Si oxide, aluminum oxide, Al nitride, Si carbide, boron nitride, etc., may be considered as materials of the filler.

Next, through holes 31 are formed in first conductive film 23A and interlayer insulating layer 22 at desired locations of insulating sheet 21, and second conductive film 23B is selectively exposed as shown in Fig. 2. Specifically, the entire surface of first conductive film 23A is coated with a

photoresist while leaving exposed the parts at which thorough holes 31 are to be formed. First conductive film 23A is then etched via the photoresist. Since first conductive film 23A is formed of Cu as the principal material, chemical etching is performed using an etching solution of ferric chloride or cupric chloride. Though the opening diameter of through holes 31 will vary according to the resolution of photolithography, it is approximately 50 to 100 μ m here. In the etching process, second conductive film 23B is covered with an adhesive sheet, etc., and protected from the etching solution. However, if second conductive film 23B itself is adequately thick and is of a film thickness with which flatness can be maintained after etching, it may be etched slightly.

After then removing the photoresist, first conductive film 23A is used as a mask to remove interlayer insulating layer 22 at parts immediately below through holes 31 by means of a laser and expose second conductive film 23B at the bottoms of through holes 31. A carbon dioxide laser is preferable as the laser. Also, if after vaporization of the insulating resin by laser, there are residues at the bottom parts of the openings, wet etching using sodium permanganate, ammonium persulfate, etc., is performed to remove the residues.

Referring now to Fig. 3, a plating film, which becomes

the multilayer connection means 14 for electrically connecting second conductive film 23B with first conductive film 23A, is formed over the entire surface of first conductive film 23A, including through holes 31. This plating film is formed by both electroless plating and electrolytic plating, and here, a Cu layer is formed to a thickness of approximately $2\mu\text{m}$ over the entire surface of first conductive film 23A, including through holes 31, by electroless plating. Since first conductive film 23A and second conductive film 23B are thereby made electrically continuous, electrolytic plating is performed using first and second conductive films 23A and 23B as electrodes to plate approximately $20\mu\text{m}$ of Cu again. Through holes 31 are thereby filled with Cu and multilayer connection means 14 are formed. Also, though Cu is employed here for the plating film, Au, Ag, or Pd, etc., may be employed instead. Also, partial plating may be performed using a mask.

First conductive wiring layer 12A is then formed by etching first conductive film 23A in desired patterns as shown in Fig. 3. First conductive film 23A is covered with a photoresist with the desired patterns, and in the case of forming wiring such as shown in Fig. 11, bonding pad parts and first conductive wiring layer 12A parts that extend to the center from the bonding pad parts are formed by chemical etching. Since first

conductive film 23A is formed of Cu as the principal material, chemical etching is performed using an etching solution of ferric chloride or cupric chloride.

In the second step of this embodiment, conductive wiring
5 layer 12 at the top surface is covered with an overcoat resin
18 while leaving exposed locations that are to become pads as
shown in Fig. 4 and Fig. 5. Referring now to Fig. 4, as overcoat
resin 18, an epoxy resin, etc., dissolved in a solvent is coated
on by screen printing and heat cured. Or, a dry film formed
10 of resin is adhered. A thermosetting resin or a thermoplastic
resin may be used as the resin to be used here. A photosensitive
resin or a non-photosensitive resin may also be used as the
material of overcoat resin 18. Furthermore, in order to expose
the conductive wiring layer at locations that are to become
15 bonding pads, the overcoat resin is partially removed at parts
above these locations.

A plating film of Au or Ag, etc., is formed in consideration
of the bonding property above the bonding pads as shown in Fig.
5. This plating film is deposited selectively onto the bonding
20 pad parts by electroless plating using overcoat resin 18 as
a mask or is deposited by electrolytic plating using second
conductive film 23B as an electrode.

In the third step of this embodiment, circuit elements

13 are affixed onto overcoat resin 18 and electrically connected with conductive wiring layer 12 as shown in Fig. 6.

Here, circuit elements 13 are semiconductor elements and are die bonded in the form of bare chips onto overcoat resin 18 by an insulating adhesive resin, etc. Since circuit elements 13 are electrically insulated from the first conductive wiring layer 12A parts immediately below by overcoat resin 18, first conductive wiring layer 12A can be wired freely even below circuit elements 13 to realize a multilayer wiring structure.

The respective electrode pads of circuit elements 13 are connected to bonding pads, which are parts of first conductive wiring layer 12A that are disposed at the periphery, by means of metal wires 15. Here, circuit elements 13 may be mounted in a face-down manner. In this case, solder balls and bumps are formed on the top surfaces of the respective electrode pads and electrodes equivalent to bonding pads are provided at parts of the top surface of first conductive wiring layer 12A that correspond to the positions of the solder balls.

In the fourth step of this embodiment, plasma is irradiated onto the top surface of overcoat resin 18, including circuit elements 13, to roughen the top surface of overcoat resin 18 while the voltage, which is charged up in overcoat resin 18, is released from conductive wiring layer 12 via conductive film

23 as shown in Fig. 7. Fig. 7(A) is a diagram showing the plasma cleaning process in outline, and Fig. 7(B) is a sectional view showing the manner in which plasma is irradiated onto a single mounting part 15.

5 As shown in Fig. 7(A), a plasma cleaner 30 has an upper electrode 31, which is disposed inside a sealed container 34, and a lower electrode 31, which is disposed opposite upper electrode 31 and on top of which insulating sheet 21 is placed. An inlet 35 for supplying gas into the container and an outlet
10 36 for exhaust the gas are also provided. One of either upper electrode 31 or lower electrode 32 is connected to a high-frequency power supply and the electrode that is not connected to the power supply is grounded.

 For plasma cleaning for removal of contaminants on the
15 top surface of the conductive foil, there are the two types of methods of chemical etching and physical etching. Chemical etching methods include the DP (Direct Plasma) and PE (Plasma Etching) methods and oxygen may be used as the gas. Physical-chemical etching methods include the RIE (Reactive
20 Ion Etching) method and an inert gas, such as argon, neon, or helium, may be used as the gas. With chemical etching, organic contaminants can be removed and the top surface can be roughened by the use of chemical effects, and with physical etching,

organic and inorganic contaminants can be removed and the top surface can be roughened by the sputter effect. Either type of method may be used with the present embodiment. Plasma irradiation using ozone may also be performed.

5 The details of surface roughening by plasma shall now be described with reference to Fig. 7(B). With this embodiment, plasma is irradiated across the entirety of insulating sheet 21. Specifically, the ions in a plasma 33, generated by discharge, are made to collide over the entirety of the top
10 surface of insulating sheet 21. Ions thus collide with overcoat resin 18, circuit elements 13, and metal wires 15 and microscopic indentations and protrusions are formed on the surfaces of these parts. Thereby, these surfaces are roughened. The organic or inorganic contaminants attached to these surfaces are also
15 removed.

Also, first conductive wiring layer 12A is electrically integral to second conductive film 23B, which is the lowermost layer. Thus even when subject to the influence of plasma, the voltage that is generated by charges accumulating in overcoat
20 resin 18 is released to the exterior via first conductive wiring layer 12A and the second conductive film. Thus even if a circuit element 13 is a CMOS, etc., which undergoes voltage breakdown readily, the damage to circuit element 13 can be restrained

to the minimum.

In the case where plasma irradiation by RIE using argon is to be performed, the ion energy of argon is set to be in the range of 40eV to 100eV. By doing so, matter attached to
5 surfaces can be removed and appropriate roughening and cleaning of the surfaces can be performed.

Furthermore, plasma irradiation can be performed by combining the DP and RIE. In this case, after performing DP using oxygen gas, RIE using an inert gas is performed. By doing
10 so, the oxide film that is formed on surfaces by the performing of DP can be removed appropriately by RIE.

Insulating sheet 21 is mechanically supported by second conductive film 23B, which is the lowermost layer. Thus even if insulating sheet 21 is heated in this step, since insulating
15 sheet 21 will undergo thermal expansion uniformly, localized thermal expansion or deformation of first conductive wiring layer 12A will be prevented. Bending and cutting of metal wires 15 due to expansion or deformation of first conductive wiring layer 12A can thus be restrained.

20 The merits of performing plasma irradiation in the state in which first conductive wiring layer 12A is covered with overcoat resin 18 shall now be described. First conductive wiring layer 12A is covered with overcoat resin 18 even at its

corner parts. The generation of sparks from corner parts of first conductive wiring layer 12A when plasma irradiation is performed can thus be prevented. Vaporization of copper, which is the material of conductive wiring layer 12A due to
5 concentration of sparks can thus be prevented. The contamination of the interior of plasma cleaner 30 by vaporized material can also be prevented.

In the fifth step of this embodiment, a sealing resin layer 17 is formed so as to cover the top surfaces of circuit
10 elements 13 and overcoat resin 18 as shown in Fig. 18.

Resin molding is performed upon setting insulating sheet 21 in a mold apparatus. Transfer molding, injection molding, coating, dipping, etc., may be carried out as the molding method. With this embodiment, resin sealing is carried out by transfer
15 molding using a thermoplastic resin. Since the top surface of overcoat resin 18 is roughened in the prior step, the adhesion of the top surface of overcoat resin 18 to sealing resin layer 17 is improved.

As shown in Fig. 8(A), insulating sheet 21 must be put
20 in flat contact with the lower die of the mold cavity in the present step, and the thick second conductive film 23B provides this effect. In addition, even after being taken out from the mold cavity, the flatness of the package is maintained by second

conductive film 23B until the shrinkage of sealing resin layer 17 stops completely. The role of mechanical support of insulating sheet 21 is thus served by second conductive film 23B until this step.

5 Furthermore in this step, blocks, in each of which a plurality of circuit elements 13 are affixed in matrix form, are formed on insulating sheet 21 and such a block is subject to unified molding in a single molding die as shown in Fig. 8(B). In this figure, a plurality of (four, in the present
10 case) blocks are disposed in a spaced manner in a single insulating sheet 21, and each block is resin sealed by a single sealing resin layer 17. A plurality of circuit devices can thus be molded using a single die, thus enabling elimination of the cost of preparing dies anew in accordance with the sizes
15 and shapes of the circuit devices to be manufactured and reduction of the amount of resin used.

In the sixth step of this embodiment, a second conductive wiring layer 12B is formed by selectively removing conductive film 23B as shown in Fig. 9.

20 Second conductive film 23B is covered with a photoresist with desired patterns to form second conductive wiring layer 12B by chemical etching. For example, second conductive wiring layer 12B are aligned at fixed intervals as shown in Fig. 11

and each part is electrically connected via multilayer connection means 14 to first conductive wiring layer 12A to realize a multilayer wiring structure.

5 A large part of second conductive wiring layer 15 is then covered with an overcoat resin 18 by screen printing an epoxy resin, etc., dissolved in a solvent, while leaving exposed the parts at which external electrodes 16 are to be formed. Then by solder reflow, external electrodes 16 are formed simultaneously at the exposed parts. Lastly, since a plurality
10 of circuit devices are formed in a matrix form in insulating sheet 21, sealing resin layer 17 and insulating sheet 21 are diced to perform separation into the individual circuit devices.

Second conductive film 23B may also be removed in an overall manner. In this case, multilayer connection means 14 are
15 exposed from the rear surface of interlayer insulating layer 11 and the external electrodes are formed at the exposed multilayer connection means 14.

The configuration of a circuit device 10 manufactured by the above-described steps shall now be described with
20 reference to Fig. 10 and Fig. 11. Circuit device 10 has an configuration comprising: first conductive wiring layer 12A and second conductive wiring layer 12B, which are laminated with interlayer insulating layer 11 interposed in between;

overcoat resin 18, which covers the first conductive wiring layer 12A; circuit elements 13, which are affixed onto overcoat resin 18 and are electrically connected to first conductive wiring layer 12A; sealing resin layer 17, which covers circuit
5 elements 13; multilayer connection means 14, which pass through interlayer insulating layer 11 at desired locations and connect the conductive wiring layers 12 to each other; and external electrodes 16, provided at desired locations of second conductive wiring layer 12B. These components shall now be
10 described.

First conductive wiring layer 12A and second conductive wiring layer 12B are formed by etching the conductive films formed on the top and rear of interlayer insulating layer 11. The conductive films are formed of a material having Cu as the
15 principal material or of a known lead frame material and may be coated onto interlayer insulating layer 11 by a plating method, vapor deposition method, or sputter method or are adhered as metal foils formed by a rolling method or plating method. Also, first conductive wiring layer 12A and second conductive wiring
20 layer 12B are covered by overcoat resin 18.

Interlayer insulating layer 11 has a function of insulating first conductive wiring layer 12A and second conductive wiring layer 12B and is disposed as a layer between

the two conductive wiring layers 12. As the material of interlayer insulating layer 11, a thermoplastic resin or thermosetting resin with the characteristic of softening at a high temperature is employed.

5 Overcoat resin 18 is formed of a thermosetting resin or a thermoplastic resin and covers a large part of first conductive wiring layer 12A. At locations that are to be pads for connection with circuit elements 13, overcoat resin 18 is partially removed and a plating film is formed. Here, the top surface of overcoat
10 resin 18 is roughened in the above-described step of performing plasma irradiation to realize firm adhesion of the roughened top surface of overcoat resin 18 to sealing resin layer 17.

Circuit elements 13 are affixed onto first conductive wiring layer 12A via an insulating adhesive agent, etc., and
15 are electrically connected to first conductive wiring layer 12A via metal wires 15. In the present embodiment, two semiconductor elements are affixed as circuit elements 13. Circuit elements besides semiconductor elements may be employed as circuit elements 13, and chip capacitors, chip resistors,
20 transistor chips, etc., may also be employed as circuit elements 13.

Multilayer connection means 14 pass through interlayer insulating layer 11 and connect first conductive wiring layer

12A and second conductive wiring layer 12B at desired locations. Specifically, a copper plating film is suited as multilayer wiring means 14. A plating film of gold, silver, or palladium, etc., may also be used.

5 Sealing resin layer 17 covers first conductive wiring layer 12A and circuit elements 13. This sealing resin layer 17 also serves the function of mechanically supporting the entirety of the completed circuit device. Sealing resin layer 17 is formed of a thermosetting resin that is formed by transfer
10 molding.

 External electrodes 16 are provided at desired locations of second conductive wiring layer 12B. That is, a large part of second conductive wiring layer 12B is covered by overcoat resin 18 and external electrodes 16, formed of soft solder or
15 other solder material, are disposed at the exposed parts of second conductive wiring layer 12B.

 An example of the planar structure of circuit device 10 shall now be described with reference to Fig. 11. The patterns indicated by solid lines are patterns of first conductive wiring
20 layer 12A and the patterns indicated by dotted lines are patterns of second conductive wiring layer 12B. First conductive wiring layer 12A forms bonding pads that surround circuit elements 13 and is disposed in two stages at parts to accommodate for

circuit elements 13 having multiple pads. First conductive wiring layer 12A is connected by metal wires 15 to electrode pads corresponding to circuit elements 13, and a plurality of parts of first conductive wiring layer 12A that are formed to fine patterns extend below circuit elements 13 and are connected via multilayer connection means 14, indicated by solid circles, to second conductive wiring layer 12B.

With this structure, even for a semiconductor element having 200 or more pads, fine patterns of first conductive wiring layer 12A can be used for extension via the multilayer wiring structure to desired parts of second conductive wiring layer 12B and connection to external circuits can be made from external electrodes disposed at second conductive wiring layer 12B.

As shown in the same figure, circuit elements 13A are mounted to first conductive wiring layer 12A at peripheral parts. Here, a chip resistor, chip capacitor, or other passive part or a bare transistor chip, diode, or other active part may be employed as circuit element 13A. By mounting circuit elements 13A at the outermost peripheral parts, the mounting density of the device as a whole can be improved.

The configuration of a circuit device 10 with a three-layer wiring structure shall now be described with reference to Fig. 12. The basic configuration of the circuit device described

with reference to this figure is the same as that described with reference to Fig. 10, and the difference lies in conductive wiring layers 12. Here, a three-layer structure, comprising a first conductive wiring layer 12A, a second conductive wiring layer 12B, and a third conductive wiring layer 12C, is formed. A large part of first conductive wiring layer 12A, which forms the conductive patterns of the uppermost layer, is covered by an overcoat resin 18. By the top surface of overcoat resin 18 being subject to plasma treatment, the top surface is made a rough surface and the adhesion of overcoat resin 18 to sealing resin layer 17 is thereby improved.

With this circuit device manufacturing method of embodiment, since plasma cleaning is performed with conductive wiring layers 12 of the entirety being made electrically integral by the lowermost layer of conductive film 23, the voltage that is generated in overcoat resin 18 by the influence of plasma can be released to the exterior via the conductive film. Damage to circuit elements 13 due to potential differences that occur as a result of the influence of plasma can thereby be restrained.

Furthermore, since the top surface of overcoat resin 18, which covers conductive wiring layer 12, is roughened by plasma irradiation, the adhesion of overcoat resin 18 to sealing resin layer 17 is improved.

Furthermore, since insulation sheet 21, with which
conductive wiring layers 12 are formed, is mechanically
supported by the lowermost layer of conductive film 23, and
the entirety undergoes thermal expansion uniformly even when
5 heated by plasma irradiation, bending and cutting of metal wires
15 due to localized thermal deformation of conductive wiring
layers 12 can be prevented.